

# Photonics in Processing



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MTO Symposium  
San Jose, CA  
March 6, 2007

Report Documentation Page				Form Approved OMB No. 0704-0188	
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1. REPORT DATE <b>05 MAR 2007</b>		2. REPORT TYPE <b>N/A</b>		3. DATES COVERED <b>-</b>	
4. TITLE AND SUBTITLE <b>Photonics in Processing</b>				5a. CONTRACT NUMBER	
				5b. GRANT NUMBER	
				5c. PROGRAM ELEMENT NUMBER	
6. AUTHOR(S)				5d. PROJECT NUMBER	
				5e. TASK NUMBER	
				5f. WORK UNIT NUMBER	
7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES) <b>DARPA</b>				8. PERFORMING ORGANIZATION REPORT NUMBER	
9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)				10. SPONSOR/MONITOR'S ACRONYM(S)	
				11. SPONSOR/MONITOR'S REPORT NUMBER(S)	
12. DISTRIBUTION/AVAILABILITY STATEMENT <b>Approved for public release, distribution unlimited</b>					
13. SUPPLEMENTARY NOTES <b>DARPA Microsystems Technology Symposium held in San Jose, California on March 5-7, 2007. Presentations, The original document contains color images.</b>					
14. ABSTRACT					
15. SUBJECT TERMS					
16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT <b>UU</b>	18. NUMBER OF PAGES <b>9</b>	19a. NAME OF RESPONSIBLE PERSON
a. REPORT <b>unclassified</b>	b. ABSTRACT <b>unclassified</b>	c. THIS PAGE <b>unclassified</b>			

# Background

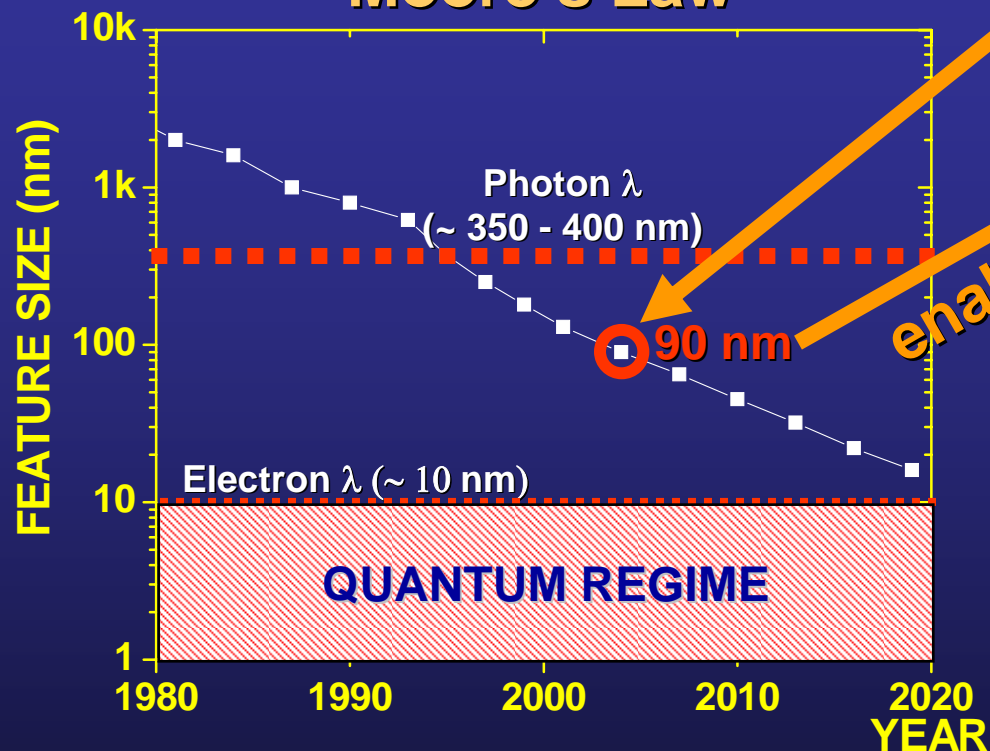
- **At DARPA since 2001**
- **Scientific Areas of Interest**
  - **Quantum Coherence/Many-body Processes in Semiconductors**
  - **Ultrafast Dynamics**
  - **Semiconductor Nanostructures (Quantum Wells, Quantum dots, Superlattices, Microcavities)**
  - **High Field Transport And Tunneling in nanostructures**
  - **Electron And Phonon Relaxation Processes (non-Markovian regime)**
  - **Physics of Photonic and Electronic Devices**
  - **Excitons and their condensates**

# Overview of Programs Developed/Managed

PROGRAM	COMMENTS
<b>CS-WDM</b> Chip-Scale WDM	<b>Photonic <u>Integration</u>:</b> Multiple WDM functions on a chip
<b>O-CDMA</b> Optical CDMA	<b>Optical <u>networks</u> with optical Code Division Multiple Access; photonic technology algorithms, systems</b>
<b>DOD-N</b> Data in the Optical Domain - Networks	<b>Optical <u>networks</u> with optical packet switching routers; aggressive photonic integration</b>
<b>EPIC</b> Electronic and Photonic Integrated Circuits	<b>Electronic/Photonic <u>Integrated</u> Circuits in silicon CMOS platform</b>
<b>UPR</b> University Photonics Research Centers	<b>Forward looking university research in photonics technologies</b>

## Electronic/Photonic Integrated Circuits

### Moore's Law



An Extraordinary OPPORTUNITY

### Silicon Nanophotonics

- Small index contrast makes current devices very large
- Large index contrast in Si/SiO<sub>2</sub> + 90 nm fab capabilities (e.g. smooth walls) → nanophotonics
- Fine Feature Size
  - Essential for very high speed

PIGGYBACK ON CMOS INFRASTRUCTURE AND PROGRESS

Silicon Nanophotonics  
+  
CMOS Electronics

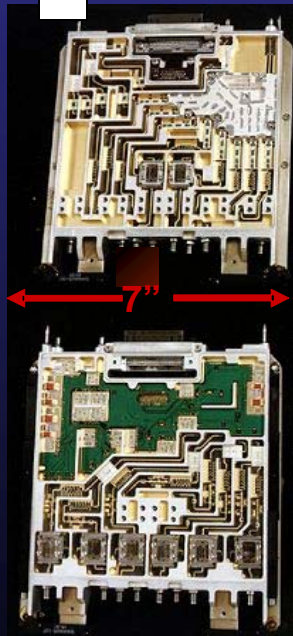
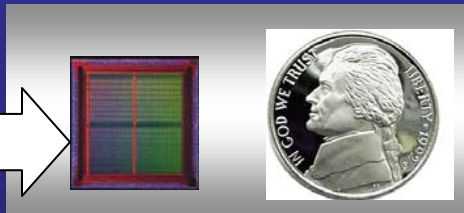
Monolithically Integrated  
VLSI Photonics and Electronics  
on a single Silicon Chip  
In a standard  
CMOS-SOI Foundry



Seamless Photonics-Electronics Interface

# Signal Processing with Integrated Photonics

**“Nickel” Size  
Optical Signal Processing  
RF Channelizer**



**4.5X Increase IBW  
95X Reduction Size  
80X Reduction in Weight  
5X Reduction in \*Power\*  
100X Reduction in Cost**



**An Example:**

**“Application Specific Electronic-Photonic  
Integrated Circuit” (AS-EPIC)  
demonstration vehicle:**

***Broadband RF Receiver (HF to Ku) using  
optical signal processing of RF signals***

- ***Dramatic SWAP reduction***
- ***Increased BW***

**Seamless Integration of Electronics and  
Photonics Will Allow Functions to be  
Combined**

- **Wide-bandwidth photonic signal processing elements can be tightly integrated with digital control circuits**
- **Open-architecture optical component library can be completely compatible with CMOS processes and foundry fabricated**

# Communications Challenge with Ultra-dense Systems

- **2D AND 3D SYSTEMS ARE BECOMING ULTRADENSE**
  - **MOORE'S LAW  $\rightarrow 10^{12}$  TRANSISTORS PER  $\text{CM}^2$** 
    - **3D ELECTRONICS**
  - **$10^{12}$  MOLECULAR UNITS PER  $\text{CM}^3$**
- **HOW DO THESE UNITS COMMUNICATE**
  - **WITH EACH OTHER?**
  - **WITH THE OUTSIDE WORLD?**

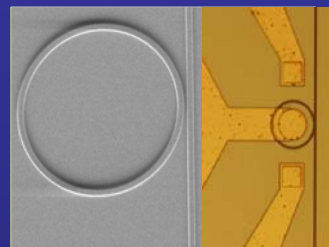
**THIS IS A FORMIDABLE CHALLENGE**

**VISION:**

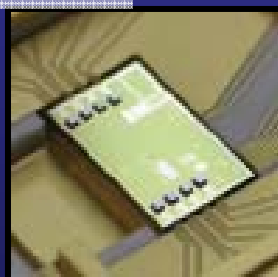
**DEVELOP A PATHWAY FOR SUCH COMMUNICATIONS**

**WHAT IS THE ROLE OF PHOTONICS?**

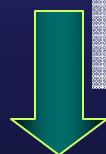




EPIC Devices



EPIC Large Scale Circuits



**EPIC TECHNOLOGY  
PROVIDES A PATH TO  
ACCESSING  
ULTRADENSE  
SYSTEMS**

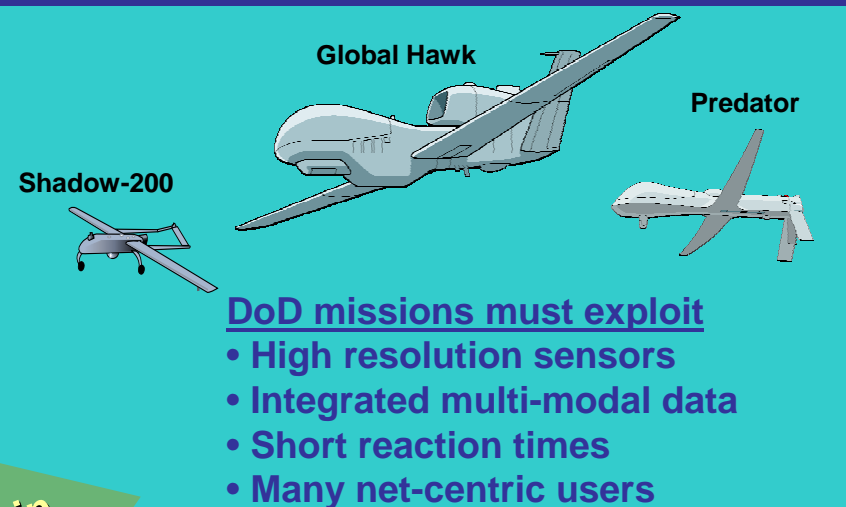
## STRATEGY

**FOCUS ON INTRA-CHIP COMMUNICATIONS ON A  
HIGH PERFORMANCE ELECTRONIC CHIP**

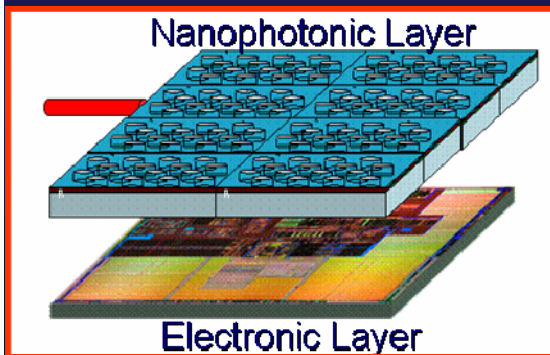
- Electronic Processor chips are faced with severe power dissipation challenges
- Wire delays, DRAM latency/BW, diminishing returns from instruction level parallelism (ILP) are forcing multi-core solutions
- Intra-chip photonic communications to enable continuation of “Moore’s law for processor performance”



- The technologies needed to realize this vision are very different from those for other optical communications (WAN, MAN, LAN etc.)
- EPIC technology can provide a path towards such technologies, but enormous challenges remain
- Such technology will also enable seamless ultrahigh performance interchip communications
- This will be a game-changing, disruptive technology



**Embedded Supercomputers in  
SWaP Challenged Systems**



**Super Supercomputers  
Exaflops, Zettaflops ...**



- Intrachip Photonic Communications: A game-changing, disruptive technology for processing
- Break down the four walls of processing
  - **Power Wall**
  - **Compute Density Wall**
  - **Memory (Latency) Wall**
  - **Productivity (Programming) Wall**
- Enormous challenges remain but programs such as EPIC have shown the path to meeting these challenges